What is claimed is:

1. An integrated circuit (IC) having functional core circuitry, comprising:

an I/O pad coupled to a first node, for providing an electrical signal to said functional core circuitry of said IC, and a first voltage line for coupling to a first voltage source;

a first electrostatic discharge (ESD) protection clamp coupled between said first node and said first voltage line; and

wherein said functional core circuitry of said IC comprises an input device, said input device comprising: a first bulk region, a source, and a drain region formed in said first bulk region and forming a channel in said first bulk region therebetween, said drain and source regions respectively coupled to logic circuitry of said functional core circuitry and said first voltage line, a gate region disposed over said channel and at least a portion of said drain and source regions, and wherein a thin-oxide gate region is disposed therebetween said gate region and said channel and said at least a portion of said drain and source regions; and

a first resistive element coupled between said source region and said first voltage line.

2. The IC of claim 1, wherein said thin-oxide gate region has a thickness less than approximately five nanometers.

3. The IC of claim 1, wherein said input device comprises a first NMOS transistor.

4. The IC of claim 3, wherein said first voltage source is grounded.

5. The IC of claim 1, wherein said input device comprises a PMOS transistor.

6. The IC of claim 3, wherein said first voltage source has a positive potential.

7. The IC of claim 1 wherein said first resistive element comprises a resistor.

8. The IC of claim 1, wherein said resistive element comprises a MOS transistor coupled in series with said input device, said MOS transistor having a drain coupled to the source of said input device, a source for coupling to said first voltage line, and a

gate for coupling to a second voltage line, said drain and source region of said MOS transistor formed in a second bulk region.

9. The IC of claim 8, wherein said gate of said MOS transistor is coupled to said second voltage line via a first resistor.

10. The IC of claim 9, wherein said first resistor has a resistance of at least 1kohm.

11. The IC of claim 8, wherein said MOS transistor is coupled to a plurality of MOS transistor input devices respectively associated with a plurality of I/O pads, said MOS transistor having said drain coupled to each source of each of said plurality of MOS transistor input devices.

12. The IC of claim 8, wherein each of the bulk regions associated with said MOS transistors are disposed over a P-substrate, said bulk regions being at least partially isolated from said P-substrate.

13. The IC of claim 12, wherein a lateral N-well ring respectively circumscribes each bulk region, thereby partially isolating each bulk region from said P-substrate.

14. The IC of claim 13, wherein a deep N-well is respectively formed between each of said bulk regions and said P-substrate, thereby completely isolating each bulk region from said P-substrate.

15. The IC of claim 12, wherein each of said bulk regions is coupled to ground via respective second resistors.

16. The IC of claim 1, further comprising a second resistive element coupled between said first bulk region and said first voltage source.

17. The IC of claim 16, wherein said second resistive element comprises one of an inductor, a resistor, and a pass-gate transistor.

18. The IC of claim 1, further comprising a second resistive element coupled from said ESD protection clamp to said source of said input device.

19. The IC of claim 18, wherein said second resistive element comprises a pass-gate transistor having a source coupled to said ESD protection clamp, a drain coupled to said source of said input device, and a gate coupled to a potential differing from said

first voltage line.

20. The IC of claim 19, further comprising a third resistive element coupled between said first bulk region and said first voltage source.

21. The IC of claim 1, further comprising a second resistive element coupled between said gate region of said input device and said first node.

22. The IC of claim 1, further comprising a second resistive element coupled between said drain region of said input device and a second voltage source.

23. An integrated circuit (IC) having functional core circuitry, comprising:

an I/O pad coupled to a first node, for providing an electrical signal to said functional core circuitry of said IC, and a first voltage line for coupling to a first voltage source;

a first electrostatic discharge (ESD) protection clamp coupled between said first node and said first voltage line; and

wherein said functional core circuitry of said IC comprises an input device, said input device comprising: a first bulk region, a source, and a drain region formed in said first bulk region and forming a channel in said first bulk region therebetween, said drain and source regions respectively coupled to logic circuitry of said functional core circuitry and said first voltage line, a gate region disposed over said channel and at least a portion of said drain and source regions, and wherein a thin-oxide gate region is disposed therebetween said gate region and said channel and said at least a portion of said drain and source regions; and

a first resistive element coupled between said first bulk region and said first voltage line.

24. The IC of claim 23, wherein said thin-oxide gate region has a thickness less than approximately five nanometers.

25. The IC of claim 23, wherein said input device comprises a first NMOS transistor.

26. The IC of claim 25, wherein said first voltage source is grounded.

27. The IC of claim 23, wherein said input device comprises a PMOS transistor.

28. The IC of claim 25, wherein said first voltage source has a positive potential.

29. The IC of claim 23, wherein said first resistive element comprises a resistor.

30. The IC of claim 25, further comprising a second input device, said second input device being a PMOS transistor comprising a second bulk region, a source and drain region formed in said second bulk region and forming a channel in said second bulk region therebetween, a gate coupled to the gate of said first NMOS transistor, a drain coupled to the drain of said first NMOS transistor, and a source coupled to a second voltage line for coupling to a second voltage source having a positive potential, said source of said PMOS device being coupled to said second voltage line, and said second bulk region coupled to ground via a second resistive element.

31. The IC of claim 30, wherein said second resistive element comprises a resistor.

32. The IC of claim 30, further comprising a second ESD protective clamp coupled between said first node and said second voltage line.

33. The IC of claim 30, wherein each of the bulk regions associated with said first and second NMOS transistors are disposed over a P-substrate, said bulk regions being at least partially isolated from said P-substrate.

34. The IC of claim 33, wherein a lateral N-well ring respectively circumscribes each bulk region, thereby partially isolating each bulk region from said P-substrate.

35. The IC of claim 34, wherein a deep N-well is respectively formed between each of said bulk regions and said P-substrate, thereby completely isolating each bulk region from said P-substrate.

36. An integrated circuit (IC) having functional core circuitry, comprising:

an I/O pad coupled to a first node, for providing an electrical signal to said functional core circuitry of said IC, and a first voltage line for coupling to a first voltage source;

a first electrostatic discharge (ESD) protection clamp coupled between said first node and said first voltage line; and

wherein said functional core circuitry of said IC comprises an input device, said input device comprising: a first bulk region, a source, and drain region formed in said first bulk region and forming a channel in said first bulk region therebetween, said drain and source regions respectively coupled to logic circuitry of said functional core circuitry and said first voltage line, a gate region disposed over said channel and at least a portion of said drain and source regions, and wherein a thin-oxide gate region is disposed therebetween said gate region and said channel and said at least a portion of said drain and source regions; and

a first resistive element coupled between said gate region and said first node.

37. An integrated circuit (IC) having functional core circuitry, comprising:

an I/O pad coupled to a first node, for providing an electrical signal to said functional core circuitry of said IC, and a first voltage line for coupling to a first voltage source;

a first electrostatic discharge (ESD) protection clamp coupled between said first node and said first voltage line; and

wherein said functional core circuitry of said IC comprises an input device, said input device comprising: a first bulk region, a source, and drain region formed in said first bulk region and forming a channel in said first bulk region therebetween, said drain and source regions respectively coupled to logic circuitry of said functional core circuitry and said first voltage line, a gate region disposed over said channel and at least a portion of said drain and source regions, and wherein a thin-oxide gate region is disposed therebetween said gate region and said channel and said at least a portion of said drain and source regions; and

a first resistive element coupled between said drain region and a second voltage source.